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CLEAN VERSION OF SPECIFICATION PARAGRAPHS

VIA-IN-PAD WITH OFF-CENTER GEOMETRY AND METHODS OF MANUFACTURE
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Serial No.: 09/751,614

The sub-title on page 1, line 3: Related Application

The paragraph beginning on page 1, line 5:

The present application is related to the following application which is assigned to the same assignee as the present application:

The paragraph beginning on page 1, line 7:

Serial No. 09/712996, entitled "Via-in-Pad Apparatus and Methods", now U. S. Pat. No. 6,429,389.

The sub-title on page 1, line 10: Technical Field

The paragraph beginning on page 1, line 11:

The subject matter relates generally to electronics packaging. More particularly, the subject matter relates to apparatus and methods for coupling the electrical contacts of an integrated circuit to bonding pads having vias.

The sub-title on page 1, line 15: Background Information

The paragraph beginning on page 4, line 15:

FIG. 4 is a perspective view of a PCB, mask, and screener, in accordance with one embodiment of the subject matter;

The paragraph beginning on page 4, line 17:

FIG. 5 is a diagrammatic top view of two lands, each having an off-center via, in accordance with one embodiment of the subject matter;

The paragraph beginning on page 4, line 19:

FIG. 6 is a cross-sectional view of the PCB shown in FIG. 4 taken along line 150 of FIG. 4, and in addition a cross-sectional view of an IC package aligned to be coupled to the PCB, in accordance with one embodiment of the subject matter;

The paragraph beginning on page 4, line 22:

FIG. 7 shows the PCB of the present subject matter being coupled to an IC package during a solder reflow operation in which adjacent solder balls are ballooning but not touching, in accordance with one embodiment of the subject matter;

The paragraph beginning on page 4, line 25:

FIG. 8 shows the PCB of the present subject matter coupled to an IC package, in accordance with one embodiment of the subject matter;

The paragraph beginning on page 4, line 27:

FIG. 9 is a top view of an IC overlying a portion of a substrate having a plurality of lands each having an off-center via, in accordance with one embodiment of the subject matter; and

The paragraph beginning on page 5, line 1:

FIG. 10 is a flow diagram of a method of fabricating an electronic assembly that includes forming off-center vias in lands to inhibit adjacent solder balls from bridging, in accordance with one embodiment of the subject matter.

The sub-title on page 5, line 7: Detailed Description

The paragraph beginning on page 5, line 8:

In the following detailed description, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific preferred embodiments in which the subject matter may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice them, and it is to be understood that other embodiments may be utilized and that compositional, mechanical and electrical changes may be made without departing from the spirit and scope of the present subject matter. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of embodiments of the present subject matter is defined only by the appended claims.

The paragraph beginning on page 5, line 18:

The present subject matter provides a solution to the problem of thermally expansive substances, such as volatile organic compounds (VOCs), outgassing during solder reflow to produce quality defects. Various embodiments are illustrated and described herein. In one embodiment, channels in via-in-pad structures are formed offset from the pad center to minimize the effect of outgassing during solder reflow. By offsetting the via channels within the pad or land, the ballooning of solder balls is significantly lessened, reducing the likelihood of adjacent solder balls touching, enabling more solder to remain in the solder joint, and reducing shear stress and shock fatigue on the land. Methods of fabrication, as well as application of the subject matter to a substrate, an electronic assembly, and an electronic system, are also described.

The paragraph beginning on page 5, line 29 is amended as follows:

In addition to the foregoing advantages, the improved via-in-pad apparatus and methods of the present disclosure are compatible with existing packaging technologies, so that significant quality improvements are achieved at a relatively low implementation cost, thus making the apparatus and methods of the present disclosure commercially competitive.

The paragraph beginning on page 9, line 12 is amended as follows:

FIG. 4 is a perspective view of a PCB 112, mask 102, and screener 103, in accordance with one embodiment of the subject matter.

The paragraph beginning on page 10, line 20:

FIG. 5 is a diagrammatic top view of two lands 130 and 131, each having an off-center via 134 and 135, respectively, in accordance with one embodiment of the subject matter. Lands 130 and 131 represent any two adjacent lands from PCB 112, and they can be similar to or identical to lands 104 (FIG. 4). Although the lands on PCB 112 can be partitioned into at least two different groups, as illustrated in FIG. 9 and discussed below, lands 130 and 131 are assumed to be from the same group of lands. Land 130 comprises a via 134, and land 131 comprises a via 135.

The paragraph beginning on page 10, line 27:

Land 130 has a geometric center 132 and an edge 138 defining a substantially circular perimeter. Likewise, land 131 has a geometric center 133 and an edge 139 defining a substantially circular perimeter. Vias 134 and 135 have geometric centers 136 and 137, respectively.

The paragraph beginning on page 11, line 10:

Although offset vias can be provided in pads or lands in a regular, orthogonal pattern, as shown in FIG. 5, embodiments of the subject matter are not to be construed as limited to such a pattern, and they can be implemented with many other types of patterns that have variations in any of the relevant variables which include but are not limited to land size, via size, relative and actual offset distance, offset angle, and pitch.

The paragraph beginning on page 11, line 16:

FIG. 6 is a cross-sectional view of the PCB 112 shown in FIG. 4 taken along line 150 of FIG. 4, and in addition a cross-sectional view of an IC package 120 aligned to be coupled to the PCB 112, in accordance with one embodiment of the subject matter. PCB 112 and IC package 120 form an electronic assembly that can be part of an electronic system.

The paragraph beginning on page 12, line 21:

FIG. 7 shows the PCB 112 of the present subject matter being coupled to an IC package 120 during a solder reflow operation in which adjacent solder balls are ballooning but not touching, in accordance with one embodiment of the subject matter.

The paragraph beginning on page 12, line 24:

When the package structure, comprising IC package 120 and PCB 112, is subjected to heat during a reflow operation, solder balls 122 become molten. In addition, any VOCs in via fill 114 within vias 115 heat up and expand. The VOCs in via fill 114 in the lower portion of via 115 are prevented from exiting downwardly from via 115 by via cap 117.

The paragraph beginning on page 13, line 23:

FIG. 8 shows the PCB 112 of the present subject matter coupled to an IC package 120, in accordance with one embodiment of the subject matter.

The paragraph beginning on page 14, line 3:

FIG. 9 is a top view of an IC 20 overlying a portion of a substrate 112 having a plurality of lands 151, 161, 171, and 181 each having a respective off-center via 152, 162, 172, and 182, in accordance with one embodiment of the subject matter. In order to avoid the possibility of asymmetric surface tension forces in the molten solder balls (122, FIG. 7) pulling IC 20 away from proper registration with lands, such as lands 104 (FIG. 7), during the solder reflow operation, the lands for any IC are arranged in two groups, so that the surface tension forces are relatively equalized.

The paragraph beginning on page 14, line 25:

FIG. 10 is a flow diagram of a method of fabricating an electronic assembly that includes forming off-center vias in lands to inhibit adjacent solder balls from bridging, in accordance with one embodiment of the subject matter. The method begins at 200.

The paragraph beginning on page 15, line 4:

In 204, a via is formed in each land. In one embodiment, the vias are formed by drilling; however, the scope of embodiments of the subject matter is not limited to drilling, and any suitable process for forming vias can be used, such as punching, microperforation, ablation, laser blasting, etching, and so forth. Each via is formed with its geometric center (e.g. geometric center 136 of via 134, FIG. 5) in a region between the geometric center and the edge of a land (e.g. geometric center 132 and edge 138 of land 130, FIG. 5). In one embodiment, no vias are drilled or otherwise formed at the geometric center of a land. However, in other embodiments vias can be formed either off-center or on-center.

The paragraph beginning on page 17, line 2:

Embodiments of the present subject matter provide significantly improved reliability of the solder connections between the electrical contacts of electronic components, such as surface mount technology components, e.g. ball grid array devices, and corresponding via-in-pad type lands on substrates, e.g., printed circuit boards. By forming the in-pad vias off-center from the geometric center of the lands, the force required for outgassing VOC's to escape ballooning solder balls is significantly lessened due to decreased surface tension and a thinner balloon wall nearer the closer sidewall of the via. This allows ballooning solder balls to vent volatile gasses more rapidly. As a result, the likelihood that adjoining solder balls can come into contact with each other is significantly reduced. Easier venting also enables a greater quantity of solder to remain in the solder joint between the IC package contacts and the substrate lands. This has the overall effect of providing stronger solder connections between the IC package and the substrate, thus ensuring greater reliability of the electronic assembly and of any electronic system incorporating such electronic assembly.

The paragraph beginning on page 17, line 17:

In addition, embodiments of the present subject matter reduce shear stresses and shock fatigue in the vicinity of the via-in-pad, because ballooning solder balls vent easier and with less force, because volatile gasses do not have to overcome as high a surface tension in the surface of the solder ball. Again, this contributes to a more reliable electronic assembly.

The paragraph beginning on page 17, line 22:

As shown herein, embodiments of the subject matter can be implemented in a number of different embodiments, including a method for fabricating a substrate, a method for fabricating an electronic assembly, a substrate, an electronic assembly, and an electronic system. Other embodiments will be readily apparent to those of ordinary skill in the art. The elements, compositions, geometry, architecture, dimensions, and sequence of operations can all be varied to suit particular product and packaging requirements.

The paragraph beginning on page 17, line 29:

The various elements depicted in the drawings are merely representational and are not drawn to scale. Certain proportions thereof may be exaggerated, while others may be minimized. The drawings are intended to illustrate various implementations of the subject matter that can be understood and appropriately carried out by those of ordinary skill in the art.

The paragraph beginning on page 18, line 4:

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the subject matter. Therefore, it is manifestly intended that embodiments of the subject matter be limited only by the claims and the equivalents thereof.